

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1. (Currently amended) A method comprising:
2 serially receiving, from a source, a plurality of forward messages each addressed
3 to one of a plurality of destinations, wherein each forward message is received at a destination
4 directly from the source;
5 receiving a plurality of availability signals, each availability signal indicating that
6 one of the destinations is available to accept a forward message;
7 simultaneously sending a forward message to each available destination;
8 simultaneously receiving, after a predetermined period of time, a plurality of
9 reverse messages from the destinations, each reverse message corresponding to one of the
10 forward messages simultaneously sent to an available destination; and
11 serially sending the reverse messages to the source.

1 2. (Original) The method of claim 1, wherein the source identifies each of
2 the forward messages by a different tag, further comprising:
3 placing a tag in a delay buffer when sending to a destination the forward message
4 identified by that tag, wherein the delay buffer implements a delay equal to the predetermined
5 period of time such that the tag is available when receiving from memory the reverse message
6 corresponding to the forward message; and
7 sending the tag to the source with the reverse message, whereby the source
8 associates the reverse message with the forward message.

1 3. (Original) The method of claim 1, further comprising:
2 associating a priority with each forward message; and

3 sending a forward message to a destination when that forward message has a
4 higher priority than other forward messages addressed to that destination.

1 4. (Original) The method of claim 3, wherein the priority of each forward
2 message represents an age of that forward message.

1 5. (Previously presented) The method of claim 1, further comprising:
2 associated a priority with each reverse message; and
3 sending a reverse message to the source when that reverse message has a higher
4 priority than other reverse messages.

1 6. (Original) The method of claim 5, wherein the priority of each reverse
2 message represents an age of that reverse message.

1 7. (Original) The method of claim 1, wherein each destination is a memory
2 bank, each forward message is a memory transaction, and each reverse message is the result of
3 one of the memory transaction.

1 8. (Currently amended) An apparatus comprising:
2 means for serially receiving, from a source, a plurality of forward messages each
3 addressed to one of a plurality of destinations, wherein each forward message is received at a
4 destination directly from the source;

5 means for receiving a plurality of availability signals, each availability signal
6 indicating that one of the destinations is available to accept a forward message;

7 means for simultaneously sending a forward message to each available
8 destination;

9 means for simultaneously receiving, after a predetermined period of time, a
10 plurality of reverse messages from the destinations, each reverse message corresponding to one
11 of the forward messages simultaneously sent to an available destination; and

12 means for serially sending the reverse messages to the source.

1 9. (Original) The apparatus of claim 8, wherein the source identifies each of
2 the forward messages by a different tag, further comprising:

3 means for placing a tag in a delay buffer when sending to a destination the
4 forward message identified by that tag, where the delay buffer implements a delay equal to the
5 predetermined period of time such that the tag is available when receiving from memory the
6 reverse message corresponding to the forward message; and

7 means for sending the tag to the source with the reverse message, whereby the
8 source associates the reverse message with the forward message.

1 10. (Original) The apparatus of claim 8, further comprising:

2 means for associating a priority with each forward message; and

3 means for sending a forward message to a destination when that forward message
4 has a higher priority than other forward messages addressed to that destination.

1 11. (Original) The apparatus of claim 10, wherein the priority of each forward
2 message represents an age of that forward message.

1 12. (Previously presented) The apparatus of claim 8, further comprising:

2 means for associated a priority with each reverse message; and

3 means for sending a reverse message to the source when that reverse message has
4 a higher priority than other reverse messages.

1 13. (Original) The apparatus of claim 12, wherein the priority of each reverse
2 message represents an age of that reverse message.

1 14. (Original) The apparatus of claim 8, wherein each destination is a
2 memory bank, each forward message is a memory transaction, and each reverse message is the
3 result of one of the memory transactions.

1 15. (Currently amended) A computer program product, tangibly stored on a
2 computer-readable medium, comprising instructions operable to cause a programmable processor
3 to:

4 serially receive, from a source, a plurality of forward messages each addressed to
5 one of a plurality of destinations, wherein each forward message is received at a destination
6 directly from the source;

7 receive a plurality of availability signals, each availability signal indicating that
8 one of the destinations is available to accept a forward message;

9 simultaneously send a forward message to each available destination;

10 simultaneously receive, after a predetermined period of time, a plurality of reverse
11 messages from the destinations, each reverse message corresponding to one of the forward
12 messages simultaneously sent to an available destination; and

13 serially send the reverse messages to the source.

1 16. (Original) The computer program product of claim 15, wherein the source
2 identifies each of the forward messages by a different tag, further comprising instructions
3 operable to cause a programmable processor to:

4 place a tag in a delay buffer when sending to a destination the forward message
5 identified by that tag, wherein the delay buffer implements a delay equal to the predetermined
6 period of time such that the tag is available when receiving from memory the reverse message
7 corresponding to the forward message; and

8 send the tag to the source with the reverse message, whereby the source associates
9 the reverse message with the forward message.

1 17. (Original) The computer program product of claim 15, further comprising
2 instructions operable to cause a programmable processor to:

3 associate a priority with each forward message; and

4 send a forward message to a destination when that forward message has a higher
5 priority than other forward messages addressed to that destination.

1 18. (Original) The computer program product of claim 17, wherein the
2 priority of each forward message represents an age of that forward message.

1 19. (Previously presented) The computer program product of claim 15,
2 further comprising instructions operable to cause a programmable processor to:
3 associate a priority with each reverse message; and
4 send a reverse message to the source when that reverse message has a higher
5 priority than other reverse messages.

1 20. (Original) The computer program product of claim 19, wherein the
2 priority of each reverse message represents an age of that reverse message.

1 21. (Original) The computer program product of claim 15, wherein each
2 destination is a memory bank, each forward message is a memory transaction, and each reverse
3 message is the result of one of the memory transactions.